

AMENDMENT UNDER 37 C.F.R. § 1.111
U.S. Application No.: 10/678,375

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. *(Currently Amended)* A modularized circuit design ~~information~~-generating tool for designing an integrated circuit having a plurality of interconnected functional modules, comprising

a circuit module design database including circuit design and corresponding specification information of functional modules of at least two categories, wherein at least one category of said functional modules includes design information of circuit modules of at least two different specifications;

an element selection means allowing a user to select suited circuit modules from said circuit module design database according to particular specifications of functional elements to be included into the integrated circuit to be designed and to include circuit design and specification information corresponding to said selected circuit modules into circuit design information file of said circuit to be designed;

a circuit module connection means to define connections between or among selected circuit modules according to features of each selected circuit module and thereby provides a circuit design of a working integrated circuit comprising said selected circuit modules;

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a memory to store circuit design information said working integrated circuit and of all selected circuit modules and information of connections between and/or among the selected circuit modules, ~~both of circuit under design or circuit as designed~~; and

a file converting means to convert the circuit design information so obtained into an applicable format.

2. *(Original)* The modulated circuit design information generating tool according to claim 1, wherein said circuit module design information database comprises a communications tool connectable to a remote database.

3. *(Currently Amended)* The modulated circuit design information generating tool according to claim 1, wherein said circuit design information database comprises a group of circuit design information filefiles for central processing unit, a group of circuit design information filefiles for processing element, a group of design information file for memory circuit and a group of circuit design information file for interfacing circuit.

4. *(Currently Amended)* The modulated circuit design information generating tool according to claim 3, wherein said group of circuit design information filefiles for central processing unit comprises core circuit design information for at least two central processing units different in operational speed, length in instruction or bus width with each other.

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5. *(Currently Amended)* The modulated circuit design information generating tool according to claim 3, wherein said group of circuit design information files for processing circuit comprises circuit design information for at least two processing elements different in function.

6. *(Currently Amended)* The modulated circuit design information generating tool according to claim 5, wherein said group of circuit design information files for processing circuit comprises circuit design information for at least one codec, at least one filter and at least one modulator.

7. *(Currently Amended)* The modulated circuit design information generating tool according to claim 3, wherein said group of circuit design information files for memory circuit comprises circuit design information for at least two types of memory different in memory space.

8. *(Currently Amended)* The modulated circuit design information generating tool according to claim 3, wherein said group of circuit design information files for interfacing circuit comprises circuit design information for at least two interfacing circuits different in function.

9. *(Currently Amended)* The modulated circuit design information generating tool according to claim 8, wherein said group of circuit design information files for interfacing circuit comprises circuit design information for at least one A/D converter, at least D/A converter, a USB interface circuit and a PCMCIA interface circuit.

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10. (*Currently Amended*) A method for designing an integrated circuit having a plurality of functional circuit module by using modularized circuit design information-generating method, comprising:

providing a circuit module design database including circuit design information of functional circuit modules of at least two categories, wherein at least one category of said functional circuit modules includes design information of circuit modules of at least two different specifications;

selecting from the design database suited functional circuit modules according to particular specifications of functional elements to be included into the integrated circuit to be designed from a circuit module design database including circuit design information of functional modules of at least two categories, wherein at least one category of said functional modules includes design information of circuit modules of at least two different specifications;

including functional circuit design and specification information corresponding to said selected functional circuit modules into circuit design information file of said circuit to be designed;

defining connections between or among selected circuit modules according to features of each selected circuit module to thereby provide a circuit design of a working integrated circuit comprising said selected circuit modules interconnected by said connections; and

converting circuit design information so obtained into an applicable format.

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11. (*Original*) The modulated circuit design information generating method according to claim 10, wherein said circuit module design information database comprises a communications tool connectable to a remote database.

12. (*Currently Amended*) The modulated circuit design information generating method according to claim 10, wherein said circuit design information database comprises a group of circuit design information ~~file~~files for central processing unit, a group of circuit design information file for processing element, a group of design information ~~file~~files for memory circuit and a group of circuit design information ~~file~~files for interfacing circuit.

13. (*Currently Amended*) The modulated circuit design information generating method according to claim 12, wherein said group of circuit design information ~~file~~files for central processing unit comprises core circuit design information for at least two central processing units different in operational speed, length in instruction or bus width with each other.

14. (*Currently Amended*) The modulated circuit design information generating method according to claim 12, wherein said group of circuit design information files for processing circuit comprises circuit design information for at least two processing elements different in function.

15. (*Currently Amended*) The modulated circuit design information generating method according to claim 14, wherein said group of circuit design information files for

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processing circuit comprises circuit design information for at least one codec, at least one filter and at least one modulator.

16. (*Currently Amended*) The modulated circuit design information generating method according to claim 12, wherein said group of circuit design information files for memory circuit comprises circuit design information for at least two types of memory different in memory space.

17. (*Currently Amended*) The modulated circuit design information generating method according to claim 12, wherein said group of circuit design information files for interfacing circuit comprises circuit design information for at least two interfacing circuits different in function.

18. (*Currently Amended*) The modulated circuit design information generating method according to claim 17, wherein said group of circuit design information files for interfacing circuit comprises circuit design information for at least one A/D converter, at least D/A converter, a USB interface circuit and a PCMCIA interface circuit.

19. (*Original*) A memory stored with circuit design information generated from the method of any of claims 10-18.

20. (*Original*) A circuit prepared with circuit design information generated from the method of any of claims 10-18.